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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,474	12/03/2003	Hidetoshi Narahara	60188-721	5418

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,474	NARAHARA, HIDETOSHI	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The meaning of the phrase "if the same description block is performed at the same time" is unclear, and renders the claim indefinite. The examiner interprets this to mean 'if the same description block is tested multiple times.'

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-7 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any concrete or tangible products.

As per claim 1, deleting a previous history of the description block does not result in a tangible product.

As per claims 2-7, analyzing the executed rows fails to produce a tangible result.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by *Hekmatpour (US Patent No. 6,523,151).*

As per **claim 1**, Hekmatpour is directed to a simulation method, comprising the steps of recording an executed-row history for each description block (column 10 lines 18-36) and\f the same description block is performed at the same time, deleting a previous executed-row history

of the description block performed at the time (column 10 lines 18-44). Hekmatpour discloses a test coverage value added analyzer that analyzes potential test coverage for a new test description to information stored in a coverage knowledge base. The information stored includes state information, transition information, and protocol information corresponding to the coverage already achieved with previously generated tests. Thus, if the new test is checking blocks of the design that have already been checked by previous tests, the analyzer is able to determine this. The test description may then be marked as redundant, and stored in a regression database.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 2-7 are rejected under 35 U.S.C. 102(b) as being anticipated by McNamara et al., herein referred to as *McNamara (US Patent No. 6,141,630)*.

As per **claim 2**, McNamara is directed to a simulation method, comprising the steps of

i. analyzing, for each description block, correspondence information that represents correspondence between combinations of input signals to the description block and executed rows (column 4 lines 28-26). McNamara discloses a test generator

that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

ii. in a simulation execution process, tracing input signals to each description block and analyzing the executed rows according to an analysis result of the correspondence information that represents the correspondence between combinations of input signals to the description block and executed rows and a trace result of the input signals to the description block (column 5 lines 11-15). During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly (column 5 lines 48-54).

As per **claim 3**, all of the limitations of the claim are taught above in claim 2, except for obtaining the trace results every unit time. McNamara is directed to the method in claim 2 wherein all changes in the signals are tracked (column 6 lines 50-59). The test generator is able to directly target transition paths, and thus is able to determine if the input results in the correct change in the signal (column 7 lines 16-36).

As per **claim 4**, all of the limitations of the claim are taught above in claim 2, except for obtaining the trace results every cycle. McNamara is directed to the method of claim 2, wherein the model is cycle-accurate (column 5 lines 60-67; column 6 lines 1-7). The model receives test vectors from the test generator and matches cycle-for-cycle the output data from the simulated design.

As per **claim 5**, McNamara is directed to an emulation method, comprising the steps of:

i. extracting, for each description block, signals used in a hardware emulation process which correspond to input signals to the description block (column 3 lines 62-64).

ii. analyzing correspondence information that represents correspondence between combinations of the signals used in hardware emulation process which correspond to input signals to the description block and executed rows (column 4 lines 28-26). McNamara discloses a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

iii. in an emulation execution process, tracing the signals used in hardware emulation process which correspond to input signals to each description block and analyzing executed rows according to the correspondence information that represents the correspondence between the combinations of the signals used in the hardware emulation process which correspond to the input signals to the description block

and the executed rows and a result of the tracing of the signals used in the hardware emulation process which correspond to the input signals to the description block (column 5 lines 11-15). During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly (column 5 lines 48-54).

As per **claim 6**, McNamara is directed to an emulation method, comprising the steps of

i. extracting, for each logic cone, signals used in a hardware emulation process which correspond to input signals to the logic cone (column 3 lines 62-64). The design block disclosed by McNamara is analogous to the logic cones in the claim.

ii. analyzing correspondence information that represents correspondence between combinations of the signals used in the hardware emulation process which correspond to input signals to the logic cone and executed rows (column 4 lines 28-26). McNamara discloses a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

iii. in an emulation execution process, tracing the signals used in the hardware emulation process which correspond to input signals to each logic cone and

analyzing executed rows according to the correspondence information that represents the correspondence between the combinations of the signals used in the hardware emulation process which correspond to the input signals to the logic cone and the executed rows and a result of the tracing of the signals used in the hardware emulation process which correspond to the input signals to the logic cone (column 5 lines 11-15). During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly (column 5 lines 48-54).

As per **claim 7**, McNamara is directed to a simulation method, comprising the steps of:

i. analyzing, for each description block, input conditions for executing respective rows included in the description block (column 3 lines 62-64).

ii. analyzing correspondence information that represents correspondence between the input conditions and executed rows (column 4 lines 28-26). McNamara discloses a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

iii. in a simulation execution process, tracing input signals to each description block and analyzing executed rows based on the correspondence information that

represents the correspondence between the input conditions and the executed rows and a tracing result of the input signal to the description block (column 5 lines 11-15). During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly (column 5 lines 48-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is 571 272 5877. The examiner can normally be reached on 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shambhavi Patel

Examiner
Art Unit 2128

SP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER